

What is claimed is:

1. A silicon on insulator structure, the structure comprising:
a handle wafer;
a single crystal silicon device layer having a central axis, a circumferential edge, a radius extending from the central axis to the circumferential edge, and a first
5 axially symmetric region which is substantially free of agglomerated intrinsic point defects; and,
an insulating layer between the handle wafer and the device layer.
2. A silicon on insulator structure, the structure comprising:
a handle wafer comprising a Czochralski single crystal silicon wafer having
two major, generally parallel surfaces, one of which is the front surface and the other
of which is the back surface of the silicon wafer, a central plane between the front and
5 back surfaces, a circumferential edge joining the front and back surfaces, a surface layer which comprises a first region of the silicon wafer between the front surface and a distance, D_1 , of at least about 10 micrometers, as measured from the front surface and toward the central plane, and a bulk layer which comprises a second region of the
10 silicon wafer between the central plane and the first region, the silicon wafer being characterized in that it has a non-uniform distribution of crystal lattice vacancies with the concentration of vacancies in the bulk layer being greater than the concentration of vacancies in the surface layer, with the vacancies having a concentration profile in which the peak density of the vacancies is at or near the central plane with the concentration generally decreasing from the position of peak density in the direction
15 of the front surface of the handle wafer;
a single crystal silicon device layer; and,
an insulating layer between the handle wafer and the device layer.

3. A silicon on insulator structure, the structure comprising:

a handle wafer comprising a Czochralski single crystal silicon wafer having two major, generally parallel surfaces, one of which is the front surface and the other of which is the back surface of the silicon wafer, a central plane between the front and back surfaces, a circumferential edge joining the front and back surfaces, a denuded zone which comprises the region of the silicon wafer from the front surface to a distance, D_1 , of at least about 10 micrometers, as measured in the direction of the central plane, and which contains interstitial oxygen, the silicon wafer being characterized in that the concentration of interstitial oxygen in the denuded zone at a distance equal to about one-half of D_1 is at least about 75% of the maximum concentration of interstitial oxygen in the denuded zone;

a single crystal silicon device layer; and,